**In order to achieve the assessment criteria (P8) you must answer the following task:**

**Task 1**

Compare between TTL and CMOS Logic families in terms of:

* Technology used.
* Power consumption.
* Speed.
* Two input **Nand** gate implementation.
* Voltage levels.

**(P8)**

**In order to achieve the assessment criteria (D3.1) you must answer the following task:**

**Task 2**

Give two different ideas to build electronic door lock using digital circuit; decide which one to be used and why?

**(D3.1)**

**In order to achieve the assessment criteria (P9 and D2.2) you must answer the following task:**

**Task 3**

Design and Construct the following combinational logic circuits:

* NAND gate using NOR gates only.
* Landing Gear Warning Circuit shown in Fig(1) ( Note: you have only NAND gates)

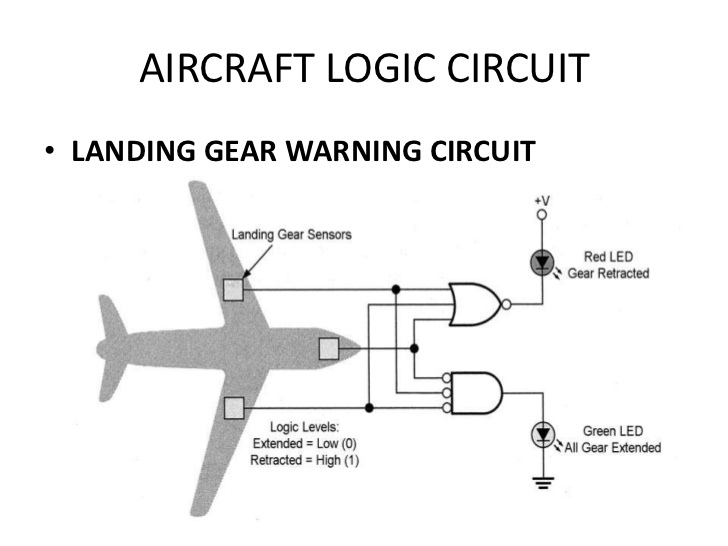


Fig (1)

**(P9 and D2.2)**

**In order to achieve the assessment criteria (P10) you must answer the following task:**

**Task 4**

Evaluate the following digital electronic circuit in terms of:

* Function.
* Operation.
* Timing diagram.

Fig (2)

**(P10)**

**In order to achieve the assessment criteria (M2.2) you must answer the following task:**

**Task 5**

Design a counter that can count in the following order (**Decide Your Count sequence**) then use your simulator software to validate your results.